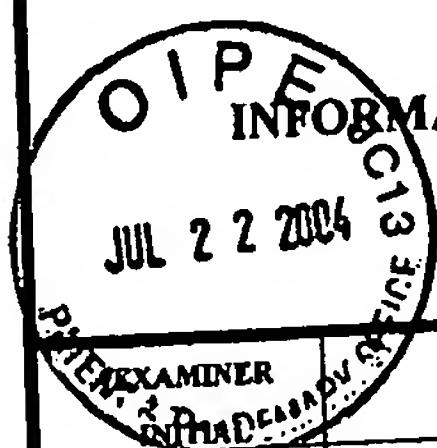


# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	CRITICAL AREA COMPUTATION OF COMPOSITE FAULT MECHANISMS USING VORONOI DIAGRAMS																																											
<p>Application Number :</p> <p>Confirmation Number:</p> <p>First Named Applicant: Robert Allen</p> <p>Attorney Docket Number: BUR920030136US1</p> <p>Art Unit:</p> <p>Examiner:</p> <p>Search string: ( 6178539 or 6247853 or 6317859 ).pn</p>																																												
<h3>US Patent Documents</h3> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>SP</td><td>1</td><td>6178539</td><td>2001-01-23</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr><tr><td>SP</td><td>2</td><td>6247853</td><td>2001-06-19</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr><tr><td>SP</td><td>3</td><td>6317859</td><td>2001-11-13</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr></tbody></table> <p><b>Signature</b></p> <table border="1"><tr><td>Examiner Name</td><td>Date</td></tr><tr><td><i>Sudhir Parikh</i></td><td>4-20-06</td></tr></table>									init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	SP	1	6178539	2001-01-23	Papadopoulou et al.				SP	2	6247853	2001-06-19	Papadopoulou et al.				SP	3	6317859	2001-11-13	Papadopoulou et al.				Examiner Name	Date	<i>Sudhir Parikh</i>	4-20-06
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INFORMATION DISCLOSURE CITATION  
(Use several sheets if necessary)

Docket Number (Optional) <b>BUR920030136US1</b>	Application Number <b>10/7096293</b>
Applicant(s) <b>Allen et al.</b>	
Filing Date <b>4-27-04</b>	Group Art Unit <b>Unknown</b>

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Papadopoulou, E. and Lee, D.T., "Critical area computation via Voronoi diagrams," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Vol. 18, No. 4, pp .463-474, April 1999.

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Papadopoulou, E., "Critical area computation for missing material defects in VLSI circuits," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Vol. 20, No. 5, pp 583-597, May 2001.

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Fook-Luen Heng and Zhan Chen. "VLSI Yield Enhancement Techniques Through Layout Modification." IBM T. J. Watson Research Center, pp. 1-15, July 17, 2000.

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EXAMINER

*Sushin Parikh*

DATE CONSIDERED

*4-20-06*

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.